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10/820,484	04/08/2004	Michael G. Kelly	10031133-1	7400

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EXAMINER	
ANDUJAR, LEONARDO	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 01/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/820,484	KELLY, MICHAEL G.	
	Examiner	Art Unit	
	Leonardo Andújar	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Acknowledgment

1. The amendment filed on in response to the Office action mailed on 11/07/2005 has been entered. The present Office action is made with all the suggested amendments being fully considered. Accordingly, pending in this Office action are claims 1-21.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims1-9 and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over anticipated by White (US 5,665,655) in view of Dias et al. (US 6,812,548).

4. Regarding claim 1, White (e.g. fig. 25) shows most aspects of the instant invention including an integrated circuit system, comprising: a die 1 incorporating an integrated circuit 2 and having a topside and a bottom side, the topside supporting an electrical signal communication metallization 6 and a topside thermal dissipation metallization 9 but does not disclose that the bottom side supports a bottom side thermal dissipation metallization. Nevertheless, Dias (e.g. fig. 5) shows a die 102 including a bottom side supporting a bottom side thermal dissipation metallization layer (e.g. gold) 128. This type of embodiment facilitates the attachment of a heat spreader

to the back surface of the semiconductor device since most of the thermal interfaces materials do not wet (i.e. stick to) semiconductors wafers (col. 2/lls. 1-14). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a bottom side thermal dissipation metallization layer in the back surface of the die disclosed by White to facilitate the attachment of a heat spreader to the back surface of the semiconductor device since most of the thermal interfaces materials do not wet (i.e. stick to) semiconductors wafers as taught by Dias.

5. Regarding claim 2, White shows that the electrical signal communication metallization comprises a plurality of exposed bonding elements on the top side of the die

6. Regarding claim 3, White shows that the bonding elements are contained in a peripheral region of the topside of the die.

7. Regarding claim 4, White shows that the topside thermal dissipation metallization is disposed in a central region of the topside of the die.

8. Regarding claim 5, White shows that the topside thermal dissipation metallization is surrounded by the plurality of boning elements.

9. Regarding claim 6, White shows that the electrical signal communication metallization surrounds the top side thermal dissipation metallization

10. Regarding claim 7, White shows that the topside thermal dissipation metallization comprises a patterned metal layer.

11. Regarding claim 8, White shows that the patterned metal layer comprises at least one through-hole 38.

12. Regarding claim 9, White shows that the patterned metal layer comprises an array of through-holes 38/39.

13. Regarding claim 21, White shows that the electrical signal communication is free of any direct electrical connection to the top side thermal dissipation metallization on the top side of the die.

14. Regarding claim 15, White (e.g. fig. 25) shows most aspects of the instant invention including a method of making an integrated circuit system, comprising: forming on a topside of a substrate 1 multiple die regions 2 each having a top side supporting and exposing an electrical signal communication metallization 6 and an exposed topside thermal dissipation metallization 9; and singulating the die regions to form respective integrated circuit dice but does not show the step of forming on a bottom side of the substrate an exposed bottom side thermal dissipation metallization for each die region. Nevertheless, Dias (e.g. fig. 5) shows a method including the step of forming on an exposed bottom side of the substrate 102 a bottom side thermal dissipation metallization (e.g. gold) 128 for each die region. This type of embodiment facilitates the attachment of a heat spreader to the back surface of the semiconductor device since most of the thermal interfaces materials do not wet (i.e. stick to) semiconductors wafers (col. 2/lls. 1-14). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the step of forming an exposed bottom side thermal dissipation metallization layer in the back surface of each of the dies disclosed by White to facilitate the attachment of a heat spreader to the back

surface of the semiconductor device since most of the thermal interfaces materials do not wet (i.e. stick to) semiconductors wafers as taught by Dias.

15. Regarding claim 16, White teaches that in each die region, the electrical signal communication metallization surrounds the top side thermal dissipation metallization.

16. Regarding claim 17, White teaches that each topside thermal dissipation metallization comprises an exposed metal layer with an array of through-holes.

17. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over anticipated by White (US 5,665,655) in view of Dias et al. (US 6,812,548) further in view of Kunikiyo (US 6,717,267).

18. Regarding claim 10, White in view of Dias shows most aspects of the instant invention except for a package comprising a top heat spreader metallurgically bonded to the topside thermal dissipation metallization of the die. Nevertheless, Kunikiyo (e.g. fig. 19) shows a top heat spreader 32 metallurgically bonded (e.g. 31) to the topside thermal dissipation metallization of the die (dummy pattern 25a). According to Kunikiyo, this type of mounting structure provides more satisfactory effect of cooling away the heat in the interlayer insulating films than conventional semiconductor devices having no dummy interconnections or dummy plugs, since metal has higher thermal conducting rate than the interlayer insulating films. This improves the circuit operation of the semiconductor device (col. 23/lls. 1-18). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include in White in view of Dias' invention a top heat spreader metallurgically bonded to the topside thermal dissipation metallization of the die such as dummy patterns in accordance to Kunikiyo's invention in

order to improve the circuit operation since the heat can be satisfactorily removed form the interlayer insulating films.

19. Regarding claim 11, Kunikiyo shows that the integrated circuit is connected electrically to the topside heat spreader by an electrical path extending through the topside thermal dissipation metallization (grounded).

20. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over anticipated by White (US 5,665,655) in view of Dias et al. (US 6,812,548) further in view of Kunikiyo (US 6,717,267) further in view of Wang (US 5,977,626).

21. Regarding claim 12, White in view of Dias further in view of Kunikiyo shows most aspects of the instant invention except for an electrical interface and a substrate containing a wiring interconnection between the electrical signal communication metallization and the electrical interface. Nevertheless, Wang (e.g. fig. 4) shows a package having a good efficiency of spreading heat and enhanced EM shielding that includes an electrical interface 28 and a substrate 20 containing a wiring interconnection between the electrical signal communication metallization and the electrical interface (col. 1/lls. 11-33; col. 2/lls. 10-14 & col. 3/lls. 10-12). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the package disclosed by Wang to package the device disclosed by White in view of Dias further in view Kunikiyo, which includes an electrical interface and a substrate containing a wiring interconnection between the electrical signal communication metallization and the electrical interface, because this package structure has a good efficiency of spreading heat and enhanced EM shielding as taught by Wang.

22. Regarding claim 13, Wang shows a top heat spreader 32 mounted on the substrate and forms a lid of the package covering the topside of the die.

23. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over anticipated by White (US 5,665,655) in view of Dias et al. (US 6,812,548) further in view of Kunikiyo (US 6,717,267) further in view of Khan et al. (US 6,853,070).

24. Regarding claim 14, White in view of Dias further in view of Kunikiyo shows most aspects of the instant invention including the teaching that a heat spreader can be metallurgicallly bonded to the back surface of a device (see Dias' fig. 6, 152) but does not disclose a structure having a second heat spreader or bottom heat spreader metallurgically bonded to the bottom side thermal dissipation metallization of the die. Nevertheless, Khan (e.g. fig. 2A) shows a bottom heat spreader 110 bonded to the bottom side thermal dissipation metallization of the die 102. According to Kahn this type of mounting structure provides an improved thermal, mechanical and electrical performance because the thermal stress is reduced due to a matched thermal coefficient (col. 1/lls. 52-67; col. 2/lls. 1-6 and col. 3/lls. 14-21). It would have been obvious to one of ordinary skill in the art at the time the invention was made to metallurgically bond a bottom heat spreader to the bottom side thermal dissipation metallization of the die disclosed by White in view of Dias further in view of Kunikiyo to improve the thermal, mechanical and electrical performance of the package as taught by Khan.

25. Claims 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over anticipated by White (US 5,665,655) in view of Dias et al. (US 6,812,548) further in view of Kunikiyo (US 6,717,267).

26. Regarding claim 18, White in view of Dias teaches further comprising mounting each singulated die in a respective package (see Dias figs. 5 and 6) but does shows the step of mounting a singulated die comprises metallurgically bonding the top heat spreader of the package to the topside thermal dissipation metallization of the singulated die. Nevertheless, Kunikiyo (e.g. fig. 19) shows the step of metallurgically bonding a top heat spreader of the package 32 (e.g. 31) to the topside thermal dissipation metallization of the singulated die (dummy pattern 25a). According to Kunikiyo, this type of mounting structure provides more satisfactory effect of cooling away the heat in the interlayer insulating films than conventional semiconductor devices having no dummy interconnections or dummy plugs, since metal has higher thermal conducting rate than the interlayer insulating films. This improves the circuit operation of the semiconductor device (col. 23/lls. 1-18). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include in the method disclosed by White in view of Dias the step of metallurgically bonding a top heat spreader to the topside thermal dissipation metallization of the singulated die such as dummy patterns in accordance to Kunikiyo's invention in order to improve the circuit operation since the heat can be satisfactorily removed form the interlayer insulating films.

27. Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over anticipated by White (US 5,665,655) in view of Dias et al. (US 6,812,548) further in view of Kunikiyo (US 6,717,267) further in view of Wang (US 5,977,626).

28. Regarding claim 19, White in view of Dias further in view of Kunikiyo shows most aspects of the instant invention but does not show that the package including a substrate a mounting step comprising the step of mounting the package substrate to the bottom side thermal dissipation metallization of the singulated die. Nevertheless, Wang (e.g. fig. 4) shows a method including a substrate 20 and the step of mounting the bottom side a singulated die 22 to the substrate. This package provides a good efficiency of spreading heat and enhanced EM shielding (col. 1/lls. 11-33; col. 2/lls. 10-14 & col. 3/lls. 10-12). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the method disclosed by Wang to package the device disclosed by White in view of Dias further in view Kunikiyo, which includes the step of mounting the bottom side a singulated die to the substrate, because this method produce a package structure having a good efficiency of spreading heat and an enhanced EM shielding as taught by Wang.

29. Regarding claim 20, White in view of Dias further in view of Kunikiyo shows most aspects of the instant invention but does not show that the top heat spreader is mounted on the substrate to form a package lid, and the step of encapsulating the die within the package with an encapsulating material. Nevertheless, Wang (e.g. fig. 4) shows top heat spreader 32 mounted on a substrate 20 forming a package lid, and the step of encapsulating the die within the package with an encapsulating material 30.

This package provides a good efficiency of spreading heat and enhanced EM shielding (col. 1/lls. 11-33; col. 2/lls. 10-14 & col. 3/lls. 10-12). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the method disclosed by Wang to package the device disclosed by White in view of Dias further in view Kunikiyo, which includes the step of mounting the top heat spreader on the substrate and encapsulating the die within the package with an encapsulating material, because this method produce a package structure having a good efficiency of spreading heat and an enhanced EM shielding as taught by Wang.

Response to Arguments

30. Applicant's arguments filed 11/07/2005 have been fully considered but they are not persuasive.

31. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

32. Applicant argues that "First, the substrate 1 disclosed in White does not constitute an integrated circuit system die. Rather, the integrated circuit system die disclosed in White corresponds to one of a plurality of regions that have been singulated from the processed substrate 1, each region of which consists of a composite structure that includes a respective portion of the substrate 1, the active region 2, and the overlying interconnect layer". This argument is not persuasive because White clearly

shows that the final product of the disclosed process is a semiconductor die (e.g. fig. 8, col. 1/lls. 14-55). Furthermore, it is noted that any integrated circuit die includes a substrate and an active area. Applicant argues the active area disclosed by White is not an integrated circuit because there is no circuit without the interconnection layers. However, this conclusion is not in accordance to general accepted meaning of active area. The active area by itself can be considered an integrated circuit because it includes plural active and passive devices connected to each other. Note that the art is interpreted in view of one having ordinary skill in the art.

33. Applicant argues that the element 6 is not supported by a top side of the die disclosed by White. Nevertheless, White's figure 25 clearly shows that the metallization 6 is supported by the top side of the die.

34. Applicant agues that the element 9 is not a top side of the metallization. Nevertheless, White's figure 25 clearly shows that the element 9 is atop the thermal dissipation metallization 6.

35. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, this type of embodiment facilitates the attachment of a heat spreader to the back surface of the

semiconductor device since most of the thermal interfaces materials do not wet (i.e. stick to) semiconductors wafers (col. 2/lls. 1-14). As it is well known in the art heat sink are used to improve the heat dissipation of the IC die in order to avoid problems associated with high temperatures within the IC such as speed problems. In addition to heat dissipation through the top side metallization layers bottom side heat dissipation would greatly improve the overall heat dissipation.

Conclusion

36. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

37. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonardo Andújar whose telephone number is 571-272-1912. The examiner can normally be reached on Mon through Thu from 9:00 AM to 7:30 PM EST.

38. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

39. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Leonardo Andújar
Primary Examiner
Art Unit 2826